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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/717,085	11/19/2003	Ramesh V. Peri	ITL1059US (P17918)	7032
21906 7590 09/18/2008 TROP PRUNER & HU, PC 1616 S. VOSS ROAD, SUITE 750 HOUSTON, TX 77057-2631				
EXAMINER BATAILLE, PIERRE MICHEL				
ART UNIT 2186		PAPER NUMBER		
MAIL DATE 09/18/2008		DELIVERY MODE PAPER		

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

# Office Action Summary

**Application No.**

10/717,085

**Applicant(s)**

PERI ET AL.

**Examiner**

Pierre-Michel Bataille

**Art Unit**

2186

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 27 June 2008.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-28 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-28 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SI/309)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_

## **DETAILED ACTION**

### ***Response to Amendment***

1. The present Office Action is responding to Applicant communication filed June 27, 2008 which followed the decision by the Board of Appeals. Claims 1, 9, 15, and 23 have been amended to further define the claimed invention. Claims 1-28 are pending in the application under prosecution.

### ***Response to Arguments***

2. Applicant's arguments with respect to claims 1-28 have been considered but are moot in view of the new ground(s) of rejection.

### ***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1-28 are rejected under 35 U.S.C. 102(e) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over US 6,728,856 (Grosbach et al).

With respect to claims 1, 9, 15, and 23, Grosbach teaches the invention as claimed, processor having an architecture that provides the processing speed advantages, the processor having an integrated microcontroller arithmetic logic unit

(ALU) 270 and a digital signal processing (DSP) engine 230 and a data/program memory 120 (see Fig. 1-2) a program memory space operable to store program instructions and data. Grosbach does not specifically teach the controller reading from the same portion of a memory line in the same cycle on two different memory buses. However, Grosbach provides the logic to have arrived that the claimed feature given the time of the invention, as the reference features allowing the capability to map at least a portion of program memory space to the data memory space in order to allow simultaneous program instruction and data access [Abstract, Col. 1, line 52 to Col. 2, Line 30]. Therefore, it would have been obvious to one of ordinary skill in the art to have arrived that the claimed feature of reading from the same portion of a memory line in the same cycle on two different memory buses because the result would have allowed program instructions processed to obtain the speed advantages of simultaneous program instruction and data access, yet provided a means to access program memory resident data without special purpose instructions, as taught by Grosbach [Col. 1, Lines 52-67].

With respect to claims 2-8, 10-14, 16-22, and 28-28, Grosbach teaches the invention that does not require two separate memories, the system providing separate data bus and separate instruction bus with a Harvard Architecture controller allowing data and instruction to be fetched simultaneously from the different memory buses; the address lines of the memory being monitored to determine if a predetermined memory location is accessed, and the memory location being mapped such that at least a

portion of program memory space to the data memory space in order to allow simultaneous program instruction and data access [Col. 1, Line 52 to Col. 2, Line 30].

### ***Conclusion***

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US 20020188813 (Boles et al) teaching on-chip hardware breakpoint generator with comprehensive memory operation detection with Harvard Architecture controller allowing simultaneous instruction and data accesses from two different memory buses..

### ***Contact Information***

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pierre-Michel Bataille whose telephone number is (571) 272-4178. The examiner can normally be reached on Mon, Tue-Fri (8:00A to 5:30P).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew M. Kim can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Pierre-Michel Bataille/  
Pierre-Michel Bataille  
Primary Examiner  
Art Unit 2186